digital

PDP-8/A
TECHNICAL SUMMARY

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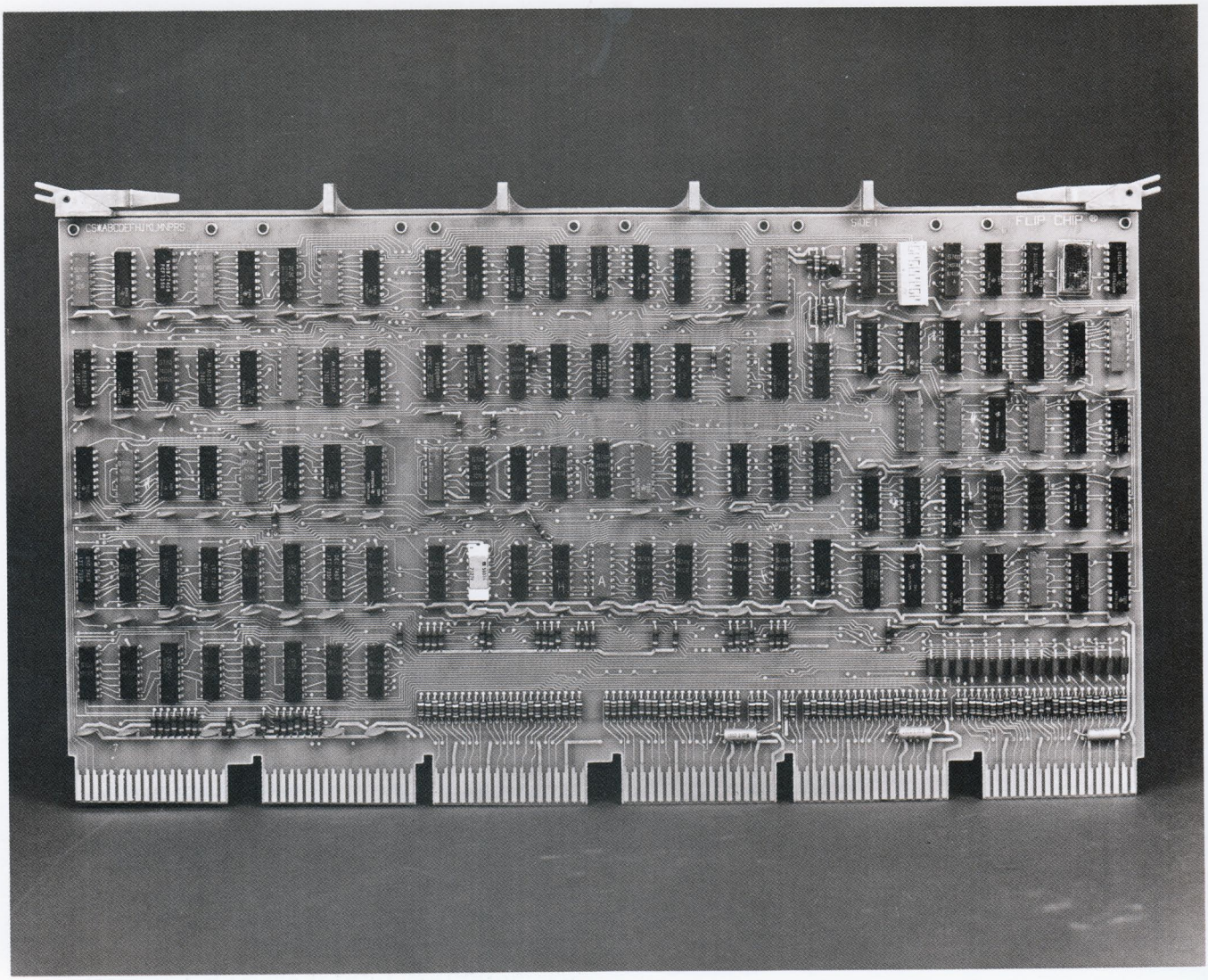
INTRODUCTION

Digital Equipment Corporation has been supplying reliable, high-performance, cost-effective computing equipment for many years. Typical is our well known PDP-8 minicomputer family. First introduced in 1965, the PDP-8 has grown in sophistication and value while decreasing in cost. New designs and efficient production techniques have helped the PDP-8 evolve into a family of compatible computers which offers the customer a choice of power, performance and price. PDP-8 market acceptance is evidenced in the 25,000-plus installations all over the world. The newest member of the PDP-8 family—the PDP-8/A—continues the tradition of increased value at reduced cost.

As an 8 family member, the PDP-8/A shares the unique OMNIBUS concept used on the PDP-8/E, F, and M. This ensures the customer the use of over 60 options and peripherals that can be directly interfaced to the 8/A. Over 600 software programs are available, including powerful program development systems like OS/8 and real-time operating system RTS-8. And the PDP-8/A utilizes proven technology, so customers can expect a high degree of reliability. Actually the 8/A is designed to exceed the present MTBF of the very reliable PDP-8/E.

Because the PDP-8/A is a compact, modular processor, customers find it easier to incorporate a computer into their application design. The choice of three memory configurations makes it possible to tailor an 8/A configuration to a particular requirement, resulting in a lower-cost solution. And the 8/A features an octal readout on the operator's console for increased accuracy and rapid interpretation. In addition to these features, the PDP-8/A is one of the fastest (1.5 μs cycle time) small computers on the market.

With the PDP-8/A, DIGITAL offers a fast, compact, reliable, inexpensive addition to the PDP-8 family that is available off-the-shelf. It's another tool with which to develop your product application with a minimum of time and expense.



CENTRAL PROCESSOR (KK8-A)

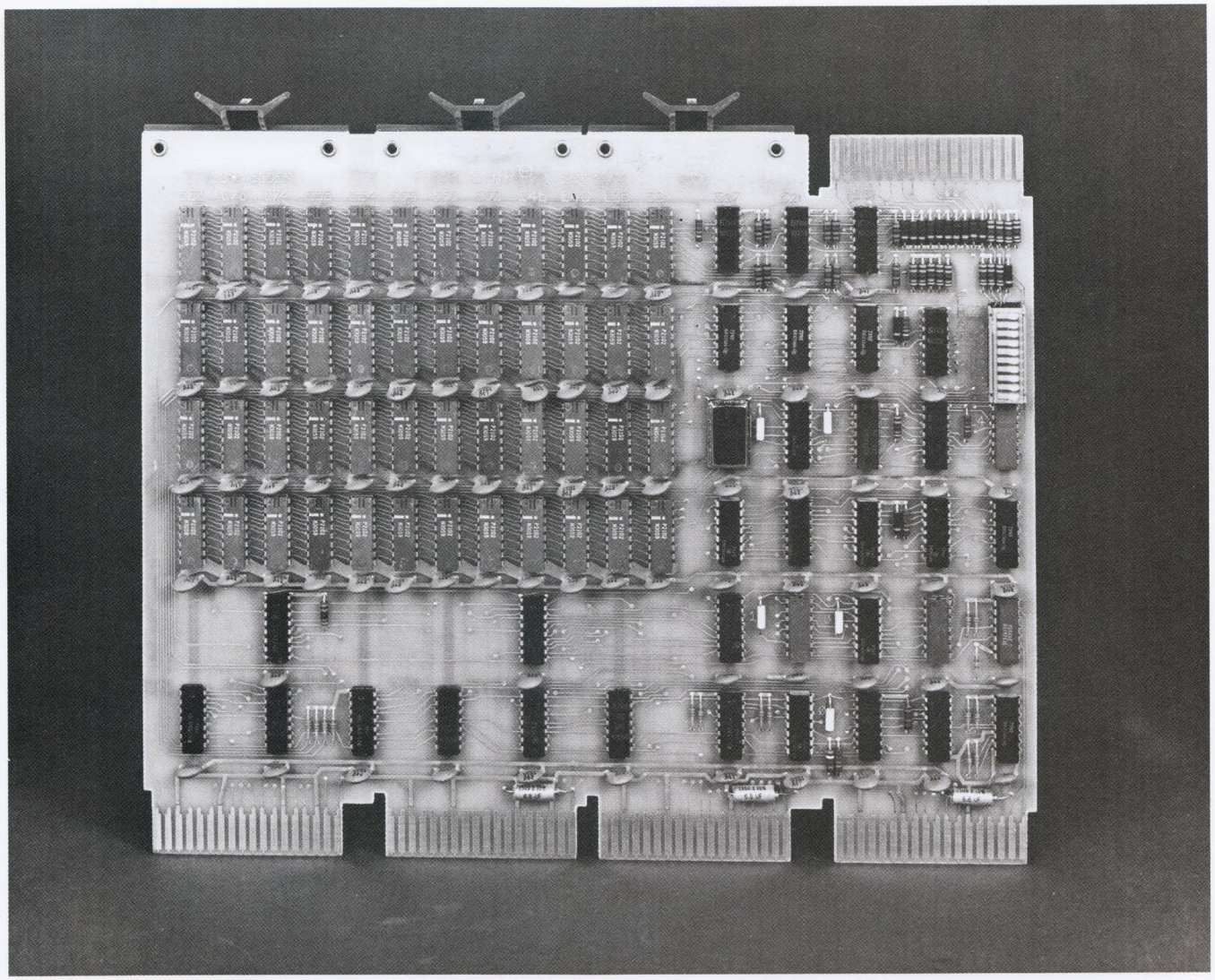
The PDP-8/A CPU is a single printed circuit card measuring 15 by 8½ inches (hex-size board). It connects to memory, option boards and other interfaces via an eight-slot OMNIBUS which gives complete hardware compatibility with PDP-8/E, F, and M peripherals (currently excepting only the AM8-E/AD8-E, MM8E, KE8-E Extended Arithmetic Element, and KP8-E Power Fail, Auto Restart). Because the CPU card includes all the bus terminations (replacing those found on the 8/E bus loads card (M8320) it can be connected to various memory board configurations and to power via the OMNIBUS to build a self-sufficient PDP-8 computer. In addition to hardware compatibility, the PDP-8/A shares the powerful PDP-8/E, F, and M instruction set for complete software compatibility.

Automatic Program Start-up

Auto-start is a standard feature of the PDP-8/A. It is initiated by asserting the OMNIBUS Power OK line (normally a power-up function). The program then starts at a predetermined address. Any one of the following locations may be selected as the starting address via switches on the CPU module: 200, 400, 1000, 2000 or 4000 of field 0. This feature works independently of the power-fail option (extended option board). When power fail is included in the configuration, a switch is available to turn auto-start off. Self starting is a particularly useful feature in "turnkey" applications.

Interface Guidelines

Because the 8/A recognizes all I/O and DATA BREAK interface signals currently available on the PDP-8/E, F, and M, the same interface guidelines for I/O, interrupt and DATA BREAK functions apply to the 8/A. (Refer to chapters 4, 9 and 10 of DIGITAL's *Small Computer Handbook*, 1974, for details.) However, note that the cycle time of the CPU is slower by a factor of 300 ns and this time difference may affect certain time-dependent PDP-8/E-type interfaces.



MEMORY

Three types of memories are available for the PDP-8/A. They are RAM, ROM and PROM.

Random Access Memory (RAM) MS8-A

General Description

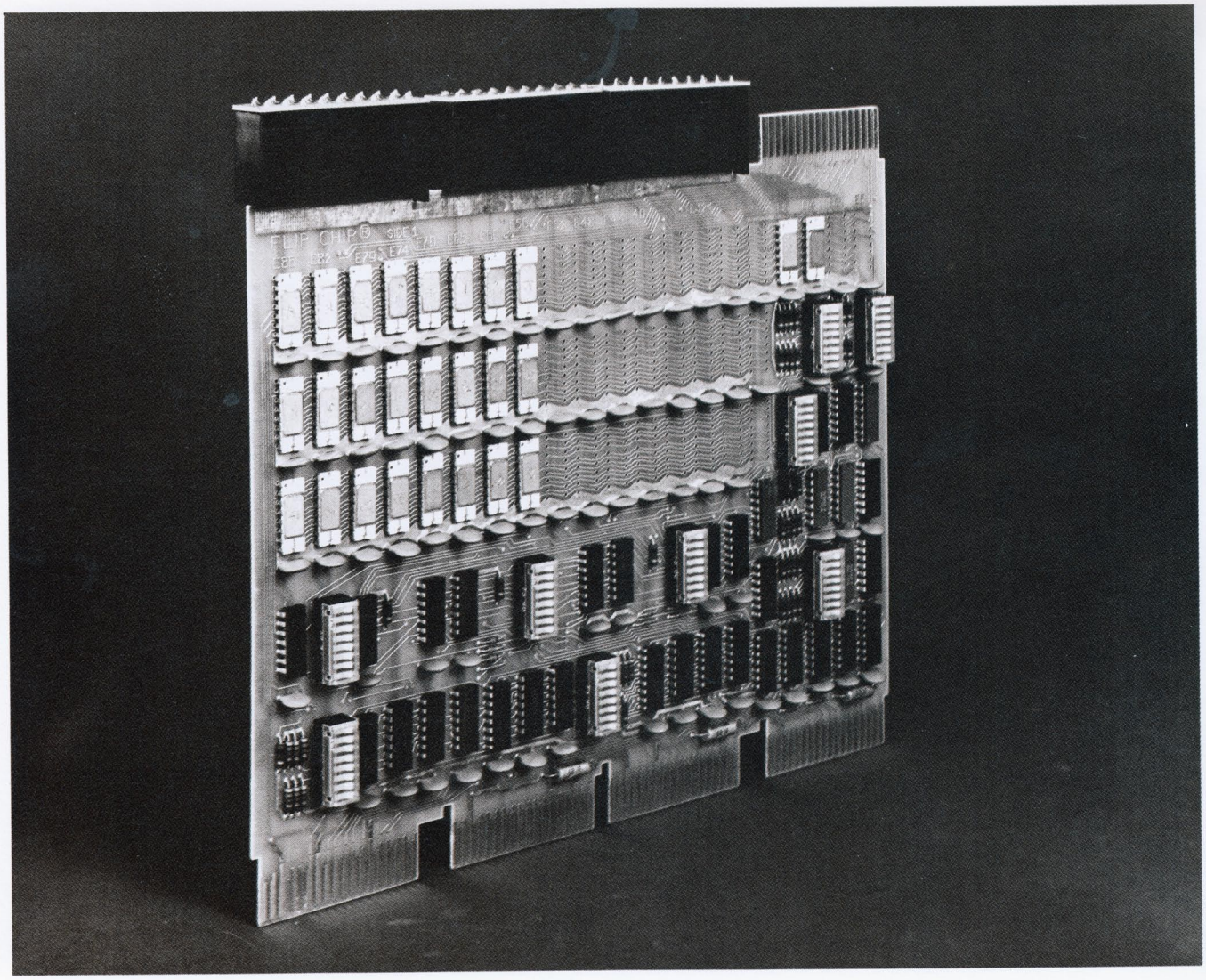
RAM memory is a printed circuit card (10 x 8½ inches, quad-size board) which uses Static MOS (1K x 1 bit) semiconductor chips requiring only +5V. RAM is read/write memory with a cycle time of 2.3 μs for a read operation and 2.8 μs for a read/write. Since the speed of RAM is slower than the processor's 1.5 μs cycle time, a memory stall signal delays the processor in its read and write time frames with RAM memory.

Three RAM memory sizes, 1K, 2K and 4K, are available and communication with the CPU is done via the OMNIBUS. However, top-connectors are also available to connect ROM and RAM combined configurations (see paragraph "RAM/ROM Configuration"). RAM can be programmed exactly like core memory.

Power

When configuring RAM combinations, include power considerations. An average of three amps is drawn by a RAM board *whether or not it is being addressed.* The power consumption table shown in the Specifications section is very useful in designing a power source.

For configurations larger than 4K of mainframe memory, the memory extension option (extended option board) must be included. Switches can be set to define both memory field and section of field (for example, on the 1K board, the 1K may be defined as locations 0000-1777, 2000-3777, etc. of any field in the range 0 to 7).



Blastable Read-Only Memory (ROM) MR8-A

General Description

ROM memory is available in 1K, 2K, or 4K capacity contained on a single printed circuit card (quad-size board, 8½ x 10 inches). ROM is organized in 12-bit width using 256 x 4 IC building blocks. It is addressed as mainframe memory and also uses a special indirect addressing scheme which allows the user to execute read/write operations in conjunction with a RAM memory. In this way, one can use RAM as scratchpad memory while a program resides in ROM.

Storage Block

The storage unit is a 256 x 4 fusible-link programmable ROM. The device is bipolar with an access time of 80 ns. It requires only +5V ±5% for operation and dissipates 0.5 mw/bit. The ROM chips are mounted in sockets for easy replacement when reprogramming or maintaining the board.

Timing

All the timing required by ROM is contained on the module itself. A standard ROM cycle is 1.5 μs and a cycle using the indirect addressing for read/write capability runs at approximately 3.0 μs.

Programming

ROM Memory allows loading of the entire memory module instead of one chip at a time (although individual chip loading is possible). The module can be loaded through the top connectors by a computer controlled Loader. The data format dictates that the user signify read/write locations and their address in RAM at the beginning of the program medium. An assembler program will be available to automatically convert core programs to ROM format. Both a Blaster/Loader and a programming service will be available to the customer.

Power

The module requires only +5V ±5% for operating and draws from 2.3 amps for 1K to 5.0 amps for 4K.

Summary

RAM/ROM Trade-Offs

RAM	ROM
Ability to Read and Write	Read only
Volatile (Data is lost when power is turned off)	Non-Volatile
Programmed like core	Loader needed to program ROM
Program not protected from write errors	Program safe from all write instructions
2.3/2.8 μs cycle	1.5 μs cycle

RAM/ROM Configuration (MS8-A/MR8-A)

DIGITAL's combined RAM/ROM memory configuration provides real advantages over configurations using RAM or ROM alone. The interconnection of ROM memory with some RAM memory gives the MR8-A read-only memory the ability to execute write instructions.

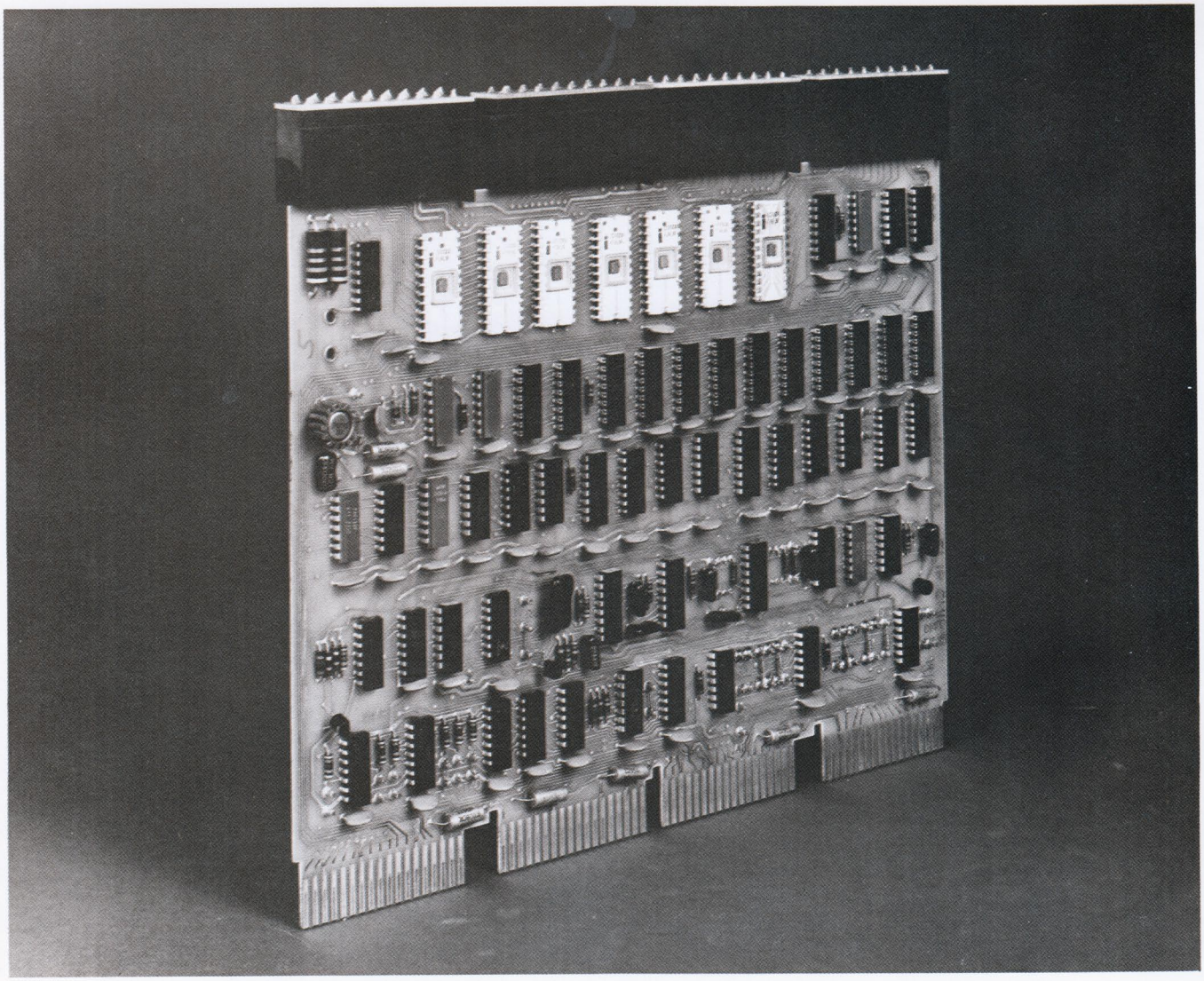
RAM can be used as scratchpad memory using an indirect addressing scheme associated with ROM. The The indirect addressing is specified by this 13th bit technique. Each location in ROM has 13 bits instead of the usual 12 bits, and the extra bit acts as a flag to the ROM hardware. Each time the 13th bit is a "0," data is accessed from ROM in the usual manner. However, when the 13th bit of the operand is set, the ROM hardware treats the 12-bit contents of the operand as an address in RAM rather than as data. This 12-bit address is sent to RAM via a top connector and it is from this address that data will be accessed or deposited. For example:

Assume that at location 200, a Deposit Accumulator instruction (DCA) is stored and the operand value is 250. (Note that DCA is a Write instruction.)

IN ROM	200 / DCA 250	Tells hardware to go to location 250.
	250 / (1)1000	At location 250, the address 1000 is stored. Since the 13th bit of the contents of 250 is set, the other 12 bits are sent to RAM.
IN RAM	1000 / AC	The address 1000 would reach RAM via a top connector and the Accumulator would be written into location 1000.

The 13th bit is inaccessible to the programmer and its use is transparent. The ROM Blaster/Loader performs the necessary hardware function of setting the 13th bit as required.

With combined RAM/ROM configurations, the advantages of both memory types are available to the customer. The main program can be stored in non-destructive ROM while the RAM can be used as scratchpad for write instructions and data storage (DMA).



Programmable Read-Only Memory (PROM) MR8-FB

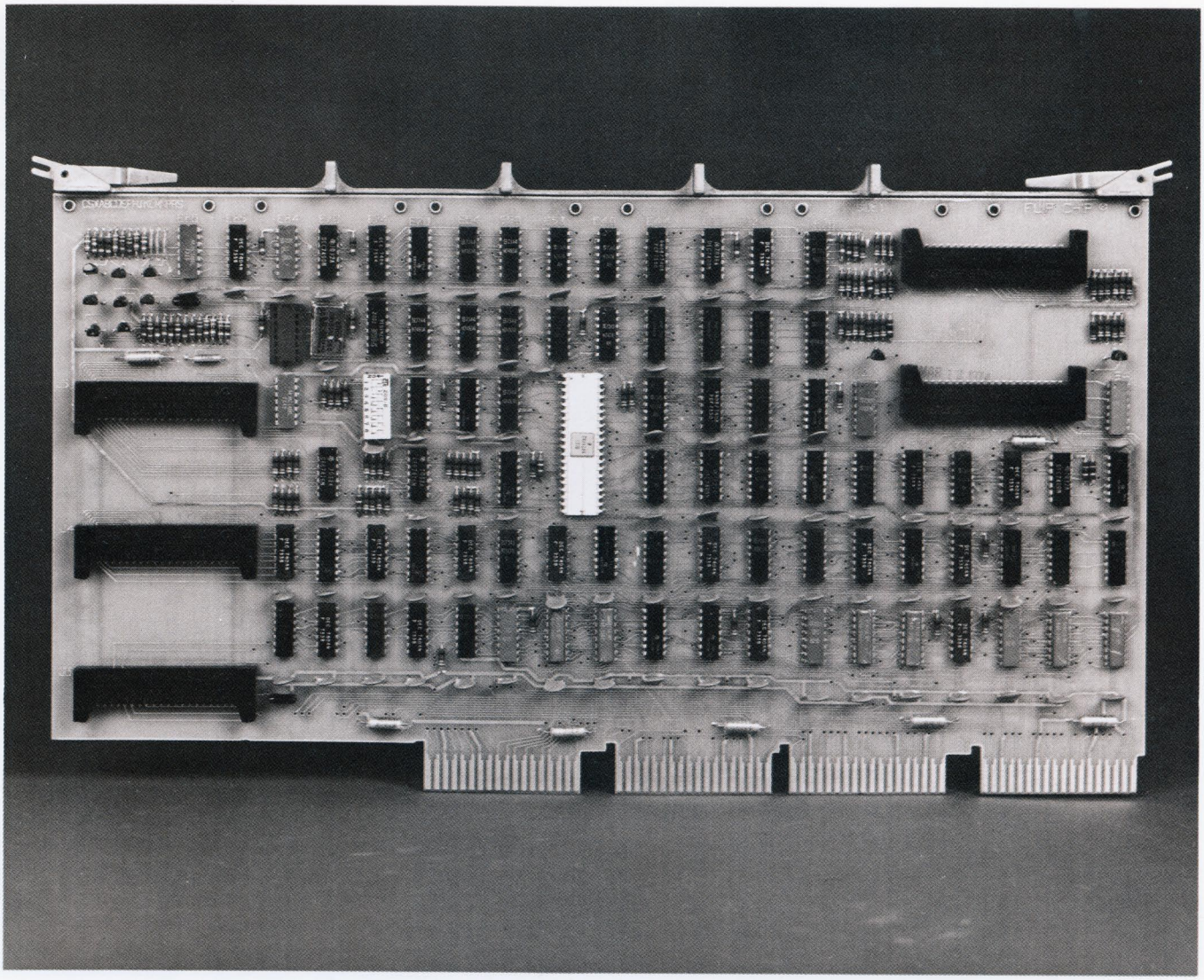
General Description

The MR8-FB is a 1K x 12-bit PROM that features read/write capability and reprogrammability (minimum of 100 times). The MR8-FB is a printed circuit card (quad-size board) which plugs into the OMNIBUS and has four top connectors. The MR8-FB contains both PROM memory and semiconductor read/write memory. Addresses can be all PROM or a combination of PROM and read/write memory. A maximum of 256 read/write locations are allowed. The cycle time of the PROM is 3.4/3.6 μsec.

PROM Chips

The MR8-FB contains seven ultra-violet erasable MOS PROM chips and assorted control circuitry. The seven MOS chips (1702A's) are housed in a 24-pin dual-in-line ceramic package. A quartz window allows exposing the chip to 2547A, 6W—SEC/CM2 ultraviolet light source necessary to erase memory contents.

See the *PROM-8M User's Guide* for detailed information.



OPTION BOARDS

I/O Option Board (DKC8-AA)

The DKC8-AA is a set of four options on one hex-size printed circuit card (15 x 8½ inches). The options included are: Serial Line Unit (SLU), Parallel I/O Interface, Real-Time Clock and Front Panel Control.

Serial Line Unit

The SLU is composed of a Universal Asynchronous Receiver/Transmitter (UART) driven by a crystal-controlled clock. The baud rate of the UART is switch-selectable as are the number of stop bits. Its device codes are fixed at 03 and 04, allowing the use of standard TTY or DECwriter software routines. Data flags and program interrupts are available to the programmer.

Specifications

Start bits	1
Data bits	8
Stop bits	1 or 2 (switch selectable)
Baud rates	110, 150, 300, 600, 1200, 2400, 4800, 9600
Device codes	03 and 04
Transmission	20 mA Current loop or EIA RS232C
Drive characteristics	20 mA—5000 feet EIA — 50 feet

Parallel I/O

The Parallel I/O Interface has the ability to transfer 12-bit words to or from the processor. Handshake-type signals are available to signal that data has been transferred. Moreover, interrupts can be generated by the data flag signals.

Specifications

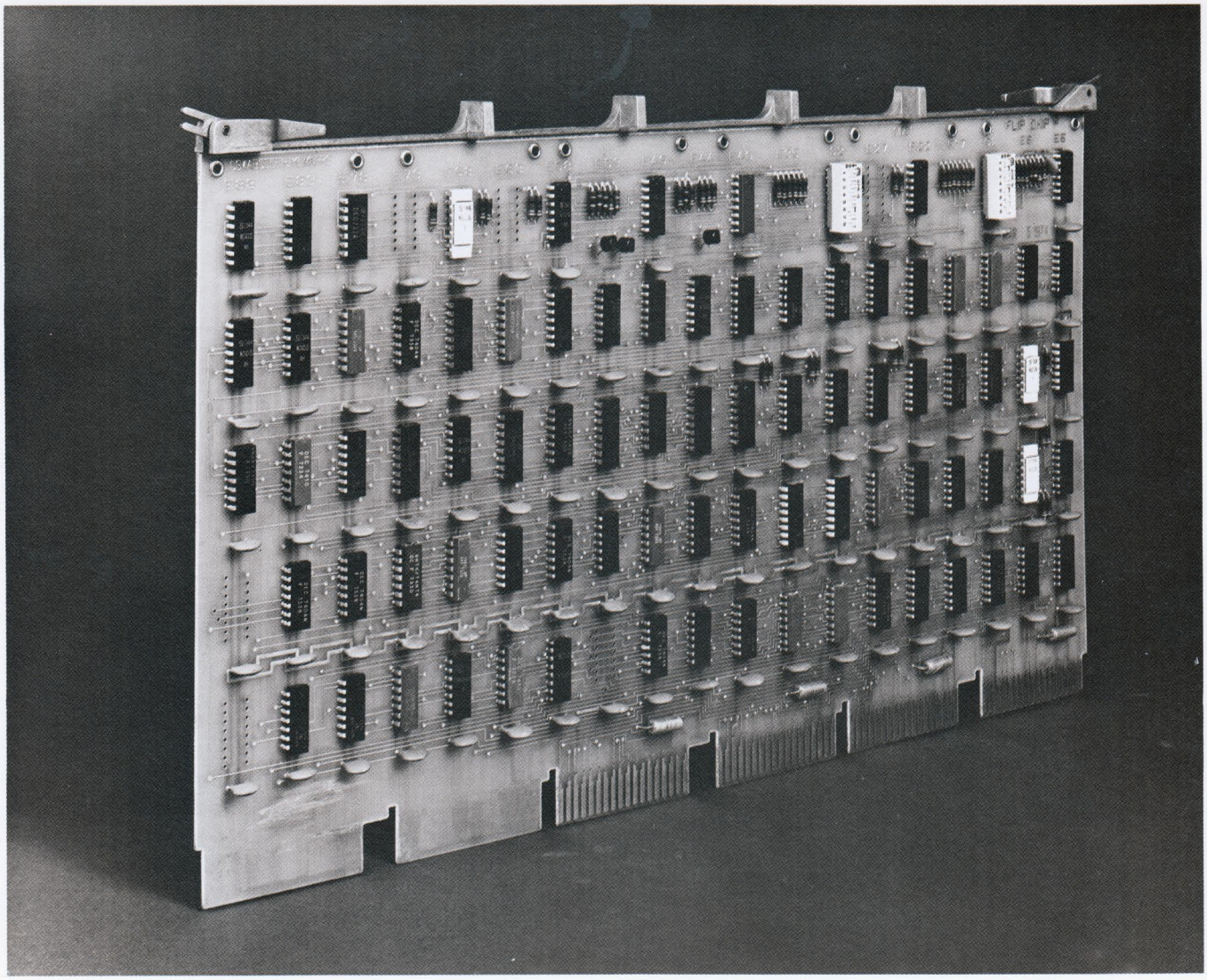
Word length	12 bits
Data flags	DATA in and DATA out
I/O levels	TTL (+5V)
Cable lengths	up to 25 feet

Real-Time Clock

The Real-Time Clock is crystal controlled and operates at 100 Hz. It provides the PDP-8/A with a hardware device that generates interrupts which may be used for synchronization or to measure time intervals. Stability is ±0.01%.

Programmer's Console Control

This option interfaces the programmer's console to the OMNIBUS. All the control signals necessary to load address, deposit, exam, etc. are sent to the CPU via this control.



Extended Option Board (KM8-A)

The KM8-A is also a hex-size printed circuit card (15 x 8½ inches) that includes Power Fail/Auto-Restart, Memory Extension Control, Time-Share Control and a 128-instruction Bootstrap Loader.

Power Fail/Auto-Restart

This Power Fail option differs from the PDP-8/E Power Fail (KP8-E) in that it monitors the ac voltage plus the dc (battery) voltage. An interrupt is developed as the ac line voltage drops. This condition is indicated by the *AC Low* signal. Furthermore, another interrupt is developed when the battery back-up is depleted. The signal *(Battery Empty)* will cause a second interrupt. These two flags give the programmer more flexibility when programming different power-fail situations. For example, when power fails, the system will switch over to battery power automatically. Prior to a Battery Empty flag being initiated, the AC Low flag can be checked again to determine if ac power has been restored. If ac power has been reestablished, the system will switch over from dc power before the batteries are completely discharged. Thereby, the program can continue operating uninterrupted.

The Auto-Restart portion automatically causes the computer to resume operation at a predetermined address when power is restored. This address is switch-selectable for Location 0000, 0200, 2000, or 4200. Additionally, a switch is available to turn off the Auto-Restart if the bootstrap loader or the CPU Auto-Start circuitry is implemented.

Memory Extension Control

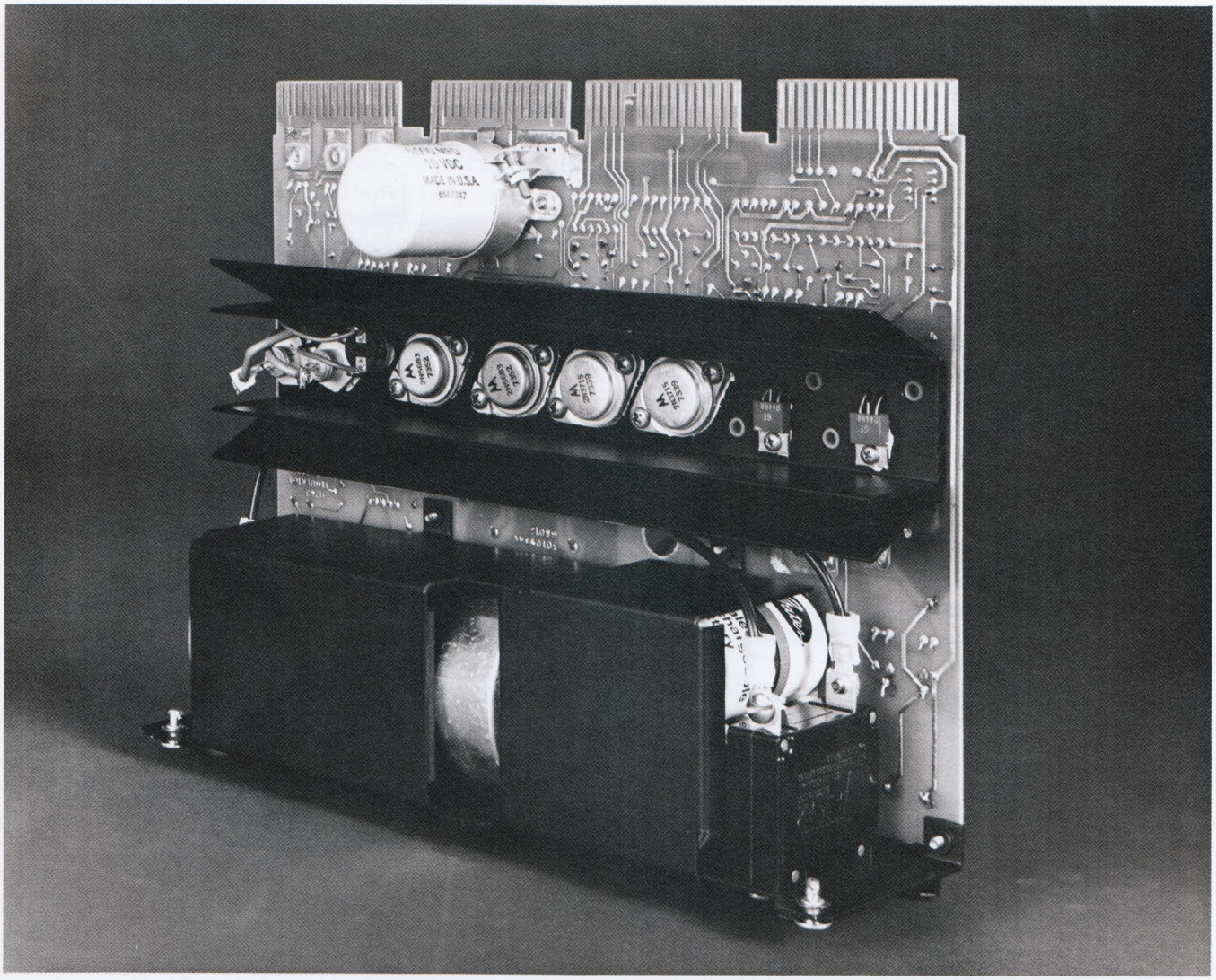
Memory Extension is required for memory configurations exceeding 4K of mainframe memory (unless the configuration is ROM/RAM combination). Example: 4K ROM and 2K RAM interfaced via top connectors, in which the RAM is used as scratchpad rather than mainframe memory. The instruction set for both the memory extension and the time-share options are the same as the PDP-8/E.

Time-Share Control

The Time-Share option provides the following:

1. Hardware to distinguish between user and monitor modes.
2. Hardware trap for certain instructions, causing an interrupt and placing the time-share system in the monitor mode. (Halts, IOTS)
3. Ability to establish user mode.

This option is required when running both TSS-8 and RTS-8 (the Time-Share and Real-Time software packages for the PDP-8).



Bootstrap Loader
The Bootstrap Loader has provisions for 128 instructions that are programmed or blasted into the same-type chips as are used on the ROM memory board. These chips may be purchased pre-blasted for five of DIGITAL's peripheral bootstraps, DECtape, RK8-E Disk, TA8 Cassette, RF08 Disk, and High/Low-speed papertape. The chips are also socket-mounted, making it possible for the user to blast the chips with his own bootstrap program. The bootstrap hardware contains an auto-start circuitry that is initiated by the boot switch on the operator's console or the AC Low signal on the OMNIBUS (a function of power-up).

CHASSIS

The PDP-8/A chassis measures 19-inches wide by 10½-inches high by 10-inches deep and includes an eight-slot OMNIBUS and fans. It is hard-mounted to the cabinet frame due to its complete front-access design. A master/slave switch is included on the chassis to define whether the computer is to control the peripheral's power or the peripheral is to control the CPU power supply.

POWER SUPPLY H763

The power regulator for the PDP-8/A is packaged on a quad-size card which plugs into a single-slot OMNIBUS-type connector. From there, the power is applied directly to the OMNIBUS via a cable harness. The quad board includes all the circuitry necessary to regulate the +5V, +15V and −15V power sources.

Additionally, the power supply includes a battery backup which allows *full* operation of the CPU and memory for a a minimum of one minute and a maximum of seven minutes. The amount of time is dependent on the memory and option configuration. (Note: 95% of all power failures are merely cycle dropouts or transients. Therefore, a one-minute battery-power phase will cover most power failures.) The battery backup is physically attached to the quad regulator board. The only component external to the regulator board is the power transformer which mounts in the chassis. Battery—8V Ni CAD.

OPERATOR'S CONSOLE

The operator's console consists of a panel, 5½ x 19 inches, that includes three switches and three indicator lights. The functions for the switches and indicators are as follows:

Switches

1. Power ON/OFF
2. Panel Lock — Used in conjunction with the programmer's console to lock out all the switches and indicators except the run light, switch register, and display function.
3. Boot — Used to Auto-Start the Bootstrap Loader on the Extended Option Board.

Indicators

1. Power ON
2. RUN
3. Battery Charging — Indicates that the battery is below charge capabilities. The light will go out when the battery is 95% charged.

The operator's console is a function panel that is included on all package units.

PROGRAMMER'S CONSOLE (KC8-AA)

The newly designed programmer's console is intended for ease of operation. The front panel switches were replaced with a 5 x 4 key pad assembly and the binary lights with LED octal readouts.

The unit also contains two examine and two deposit functions. One pair of functions allows the user to examine or deposit into a location *without* automatically updating the memory address. This allows an examine and redeposit of correct data without having to perform multiple-load address functions. The second pair of exam/deposit functions automatically increments the MA after each depression of the key.

Another new feature is the elimination of the single-instruction function. Only single step (HALT at the end of each major state) is possible. The HALT/SS Key accomplishes the same results as the HALT key used in conjunction with the continue key on the PDP-8/E. The PDP-8/A can be started via an ON/OFF toggle switch which is located on the operator's console. Also included is a PANEL lock switch. When this switch is on, the only functions that will work are the load SW Reg, DISP, and the RUN light.

The switch register is located within the logic and must be loaded in a manner similar to LOAD ADDR. The switch register is cleared on power on, but is not cleared by INIT. Since the switch register is a hardware register, it is lost in a power-down situation.

The programmer's console may be located up to 15 feet from the central processor. It requires the I/O option board to interface to the OMNIBUS. The following is a description of the switches and indicators for the programmer's console:

Indicators

RUN — The Run Indicator is lighted to show that the "Run" Flip-Flop is set and the machine timing is running. Certain panel functions are not allowed when the run flip-flop is set.

ADDRESS — The five seven-segment readouts show the content of the 3-bit "EMA" bus and the 12-bit "MA" bus. These five digits show the current address of the memory being accessed. (This is different from the 8/E, as the 8/E showed the next memory location to be accessed.)

CONTENT — The four seven-segment readouts show the contents of the register corresponding to the indicated display. If all the display indicators are out, the entry is being displayed in the content.

Display Indicators

The seven display indicators show which register is being displayed in the content register. If all the indicators are out, the entry is being displayed. The following are the registers and their content:

"AC" — The contents of the accumulator at time-state 1 are displayed.

"MQ" — The contents of the multiplier quotient at time-state 1 are displayed.

"BUS" — The contents of the 12-bit data bus (DATA0-11) at time-state 1 are displayed.

"STATUS" — The status information at time-state 1 is displayed.

"SR" — The contents of the switch register is displayed.

"STATE" — The state registers are displayed.

"MD" — The contents of the 12-bit memory bus (MD0-11) is displayed.

Keyboard

GENERAL — The twenty-button keyboard can be considered to be divided into two sections—the eight numbers (0 to 7) and the twelve functions. If the last button pushed was a function button, then the first number button pushed is entered into the right-most digit of the entry and the remaining digits are cleared to zero. Each succeeding number will cause the entry digits to be shifted to the left one digit, and that number will be entered into the right-most digit.

"RUN" — Pressing the "RUN" button generates a Mem start L signal which sets the run flip-flop and the machine begins the program at the address that is in the CPMA.

"LSR" — Pressing the "LSR" (Load Switch Register) button loads the entry into the switch register.

"HLT/SS" Pressing the "HLT/SS" (Halt or Single Step) button while the machine is running will cause the machine to stop at the end of the next machine cycle. If the machine is stopped, pressing this button will cause the machine to execute one machine cycle.

"DISP" Pressing the "DISP" (Display) button will load the right-most digit of the entry into the display register. The register corresponding to the number will then be displayed in the content readouts. For the convenience of the operator, the name of the register is written above the number on the front panel.

"BOOT" Pressing the "BOOT" button will cause the switch flip-flop to toggle. If the switch flip-flop is set, it will assert the SW line on the OMNIBUS. To perform a bootstrap operation, the boot button must be pressed twice. Note: This signal from the programmer's console is ORed with the boot switch on the operator's console and either one can hold the SW line asserted on the bus.

"E THIS" Pressing the "E THIS" (Examine This) button displays in the content the data in current address without automatically incrementing CPMA and PC.

"E NEXT" Pressing the "E NEXT" (Examine Next) button does the same as "E THIS" except that the CPMA and PC are incremented afterwards.

"D THIS" Pressing the "D THIS" (Deposit This) button loads the contents of the entry into the MB register and into memory at the address specified by the CPMA register. However, the CPMA and the PC are not incremented.

"D NEXT" Pressing the "D NEXT" (Deposit Next) button does the same as "D THIS" except the CPMA and PC are incremented.

"LA" Pressing the "LA" (Load Address) button loads the content of the entry into the CPMA and enables the fetch major state for the next processor cycle.

"LXA" Pressing the "LXA" (Load Extended Address) button loads the right-most digit of the entry into the data field register, and the next digit into the instruction field register.

"INIT" Pressing the "INIT" button generates an initialize pulse that clears the AC, Link, all I/O flags and all interrupt flip-flops to zero.

POWER CONSUMPTION

	+5V (Amps) Quiescent	+5V (Amps) Operating	+15V (Amps)	−15V (Amps)
Processor (M8315)	5.0	5.0		0.040
RAM (M8311) 1K	2.0	2.0		
2K	2.0	2.0		
4K	3.2	3.2		
ROM (M8312) 1K	2.0	2.0		
2K	3.1	3.1		
4K	5.0	5.0		
I/O Option Board (M8316)	2.0	2.0		0.1
Extended Option Board (M8317)	2.0	2.0		
MR8-FB PROM	3.8			0.35

Programmer's Console—Power supplied by I/O Option Board and adds 1.8A to the I/O Option Board current requirements.

Operator's Console—Obtained directly from power supply. Requirement negligible.

NOTE: With the H763 Power Supply, only memory configurations of up to 16K are possible because of current limitations.

Programmer's Console—Power supplied by I/O Option Board and adds 1.8A to the I/O Option Board current requirements.

Operator's Console—Obtained directly from power supply. Requirement negligible.

NOTE: With the H763 Power Supply, only memory configurations of up to 16K are possible because of current limitations.

POWER SUPPLY SPECIFICATIONS

Input

90-135 volts	H763-A
180-270 volts	H763-B

50 ± 1 Hz
60 ± 1 Hz

Output

Voltage	Current	Ripple
+ 5V ±2%	20A	50 mV
−15V ±5%		500 mV
+15V ±5%	sum=1A	500 mV

Over voltage protection—5.6 to 6.2V on the +5V line.

Power Consumption

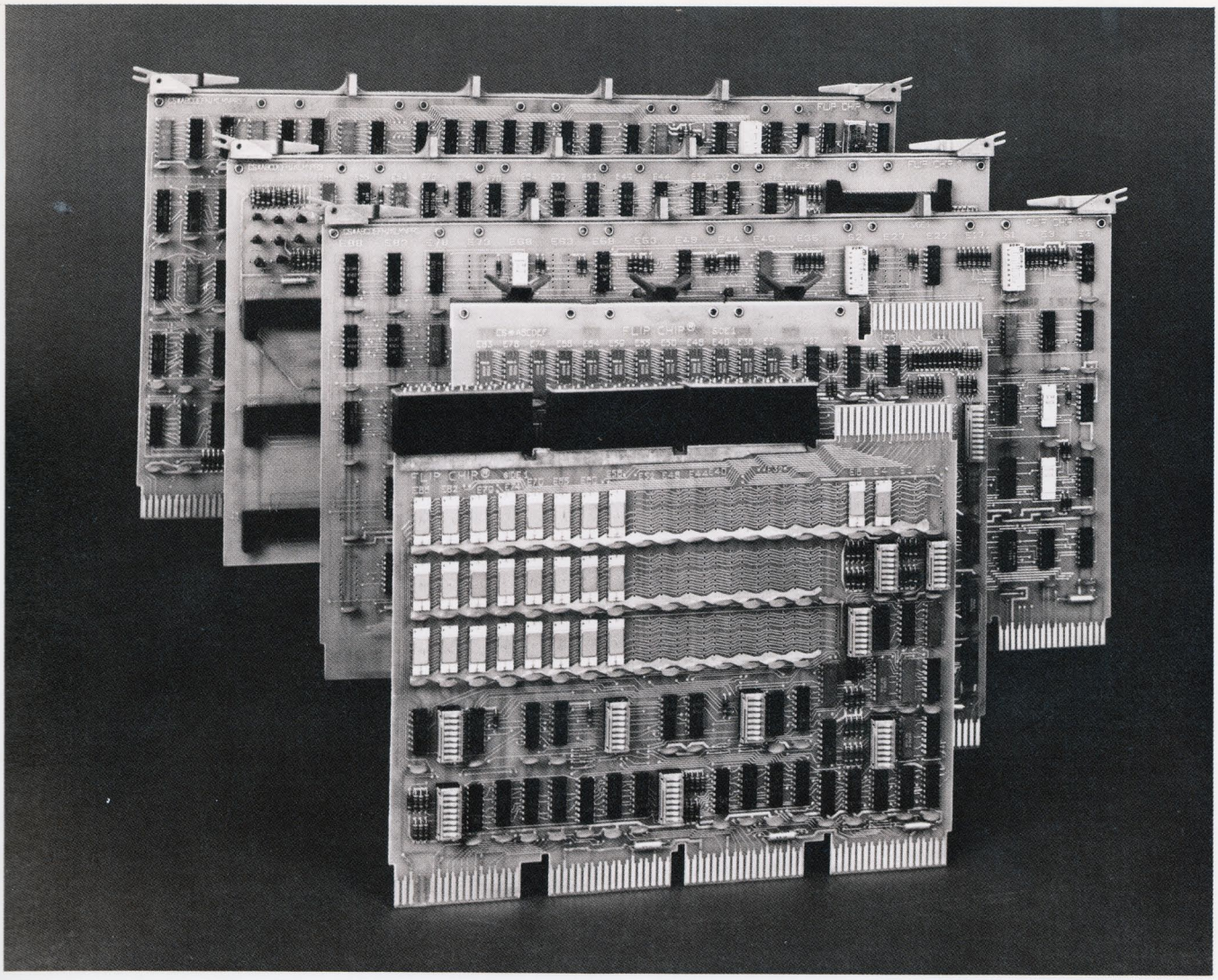
3A for 117V Full load
2A for 220V Full load

Power requirements for the individual boards are stated in the power consumption table in the Specification section.

The power transformer is included with the regulator board as a self-contained power source and is mounted in the chassis.

PDP-8/A PRODUCT SPECIFICATIONS

Word Length:	12 bit	
Cycle Time:	1.5 μs	
Hardware Registors:	2 (AC and MQ)	
Auto-Index Registors:	8 (Loc 10-17) Operating Times	
Memory:	RAM 1K, 2K, 4K	2.3 μs
	ROM 1K, 2K, 4K	1.5 μs
	PROM 1K	3.4 μs
Memory Expansion:	Up to 32K (see Power Consumption Chart)	
Input/Output:	Programmable and interrupt-driven I/O. Direct memory access via DATA BREAK for high-speed data transfers (667,000 words/sec).	
Addressing Capability:	1 instruction may address 256 locations directly/4096 indirectly.	
Instruction Set:	Same powerful instructions as the PDP-8/E.	
Software:	Complete compatibility with the PDP-8 Family software to include OS/8, CAPS-8, RTS-8.	
Instruction Execution Time: (Assumes 1.5μs memory times)	Add	3.0 μs
	AC—Mem.	3.0 μs
	Zero AC	1.5 μs
	Input DATA	1.5 μs
Options:	Two option configurations are available on hex boards.	
DKC8-AA (I/O Option Board)	KM8-A (Extended Option Board)	
Front panel control Serial line unit Parallel I/O Real-time clock	Power Fail/Auto Restart Memory Extension Bootstrap Loader	
Physical Size:	CPU on one hex board—15½ inches x 8½ inches Memory on one quad board—8½ inches x 10½ inches Box 10 inches x 10½ inches x 19 inches	
Operating Environment:	Ambient Temperature 5-50°C Relative Humidity 8-90% (non-condensing)	



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